REMARKS:

The Official Action of November 30, 2007 has been reviewed. Without necessarily agreeing with the examiner's comments as to the "adapted to" language of claims 3 - 8, claims 3 - 8 have been amended to eliminate the "adapted to" language. The examiner's comments therefore no longer apply.

Claims 1 - 10

Claims 1 - 10 stand rejected under 35 U.S.C. § 102(b) as anticipated by the U.S. patent No. 5,745, 351 of Taurand. To anticipate, a reference must meet every element of the rejected claim. Applicant's response filed October 2, 2007 pointed out how the Taurand patent differed from claim 1. The outstanding Official Action makes no mention of applicant's prior discussion in this respect.

It is noted that at page 3, line 1 of the outstanding Official Action, the examiner refers to "Levran et al." Applicant understands this to be an error and that the remainder of the particular paragraph in the Official Action relates to the Taurand patent. There is no Levran et al. reference of record in the application.

The Official Action states that the reference discloses "a power transformer ..., a first semiconductor switch ..., a first control circuit ..., a second control circuit ..., a current sensor ...." To that point the Official Action is correct. However, claim 1 calls for:

> at least one of the first and second control circuit having a current sensor for detecting the direction of current through the semiconductor switch controlled by that control circuit and enabling the turning ON of that semiconductor switch when a reverse current through the semiconductor switch is detected. (Emphasis supplied.)

The Taurand patent relates to a DC-DC converter with control circuits for switches in the primary and the secondary circuits. In col. 6, lines 27 - 31, Taurand describes how the switching on and off in the secondary is controlled:

> Advantageously, the duration of the secondary period is calculated from a set of parameters including at least a parameter corresponding to the supply voltage, a parameter corresponding to the output voltage of the converter, and a value of a maximum current at the output of the converter.

In col. 6, lines 38 - 42, Taurand describes how the switching on and off in the primary is controlled:

> Advantageously, the duration of the primary period is determined by the switching off of the first switch, which is triggered when a current in the primary circuit is higher than a control signal depending upon the difference between the output voltage of the converter and a reference voltage.

As for turning on the secondary switch Ts, Taurand explains that the switch Ts is turned on at the end of a period "T4" (Fig. 4a and 4e). Taurand states:

> At the end of T4, the circuit 80 provides circuit 70 with a signal S(T') indicating the end of the period T4, which triggers the next cycle by switching on Tp. (Col. 12, lines 18 - 21.)

The time T4 is determined by a delay line 83 (Fig. 12) providing a delay after the period T3 ends. Taurand states:

> This is the end of period T3. A voltage rising edge provided by the Output $\overline{Q}$ of the flip-flop 81 is transmitted in the delay line 83 until it reaches flip-flop 71 with a delay T4'. This rising edge corresponds to the signal S(T4') and causes a new cycle to startup. (Col. 14, lines 59 - 64.)

And the period T3 is the period during which the secondary switch Ts is ON, which is determined by "counting." Taurand says:

> When counting of T3 is ended, the circuit 80 switches off switch Ts , which corresponds to the beginning of period T4. (Col. 12, lines 16 - 18.)

No switching on of a switch in Taurand is determined by sensing a reverse current in that switch as called for in claim 1.

In the Official Action there is a reference to "a reverse current" column 12, lines 30 - 65 and column 13, lines 1 - 50. These selections from the Taurand patent do not suggest detecting "the direction of current through the semiconductor switch ... and enabling the turning ON of that semiconductor when a reverse current through the semiconductor switch is detected." At no place does Taurand describe detecting reverse current flow in a semiconductor switch to determine that switch should be turned on as called for in claim 1. The Taurand patent thus does not anticipate claim 1. The rejection, then, is in error and should be withdrawn.

Claims 2 - 10, by their dependencies, differ from the Taurand patent in the same way as claim 1. The rejection of these claims as anticipated by the Taurand patent is also in error and should be withdrawn.

Addressing claim 2, the outstanding Official Action states, "in regards to claim 2, (column 19, 35 - 55), voltage across the switch is zero volts (column 10, line 1 - 20)." This statement is not understood. Claim 2 does not call for voltage across a switch being zero. It is thought that perhaps a typing error has occurred as col. 19, lines 35 - 55 is unrelated to the remainder of the statement. Clarification is requested.

From the foregoing discussion of how Taurand controls its switches TP and TS it should be apparent that Taurand does not teach the features of claims 2 - 10. The rejection of these claims as anticipated by Taurand is in error for this reason as well as by their dependency and should now be withdrawn.

Claims 11 and 12

The outstanding Official Action states no rejection of claims 11 and 12, so these claims should be allowed. Moreover, from the above discussion of Taurand and the following discussion of the other art relied upon in the outstanding Official Action, it will be apparent that the features of claims 11 and 12 are not taught or made obvious by the art of record and should be allowed.

Claims 21 - 27

Claims 21 - 27 stand rejected as anticipated by the Martin U.S. patent No. 5,109,326. Independent claim 21 requires "at least one of the first and second control circuits (for the switches in the primary and secondary) being responsive to a reverse current through the switch controlled thereby to turn on that switch at substantially zero voltage across it." This cannot be found in the Martin patent and so this rejection is not well taken.

At col. 2, lines 9 - 21, Martin states an operation clearly contrary to claim 21:

> Also, the primary control circuit is magnetically coupled to the core, such that it initiates each ON state of the primary transistor in response to a flux decrease in the core caused

by the secondary transistor turning OFF: and, the secondary control circuit is magnetically coupled to the core such that it initiates each ON state of the secondary transistor in response to a flux decrease in the core caused by the primary transistor turning OFF. A range of input voltages and output voltages is achieved by ratioing of the ON time of the primary transistor to the ON time of the secondary transistor.

Claims 22 - 27 are dependent claims. By their dependency they incorporate the subject matter of claim 21. For that reason, as well as for their further content not taught by Martin, the rejection of these claims should be withdrawn.

Claims 13 - 20

Claims 13 - 20 stand rejected as unpatentable over the U.S. patent to Faulk et al, number 5,841,641, and Pietkiewicz et al., U.S. patent number 5,539,630. While the Faulk power converter does appear to have current and voltage wave forms similar to those of the present invention, the Faulk circuit does not self-regulate by controlling the duty cycle in response to output voltage. The Pietkiewicz converter has output voltage regulation but not by variation of a duty cycle which, in the Pietkiewicz patent, is fixed at substantially 50%. Col. 6, lines 52 - 57. Consequently these two patents cannot be combined in any obvious way to arrive at the claimed invention. The rejection is in error and should be withdrawn.

The outstanding Official Action states, "Faulk disclose the claimed subject matters a DC-DC converter (figure 3A-B), including self-regulation (column 30, line 35 - 40 ...." However, claim 13 refers to self-regulation with respect to output voltage, while the regulation referred to by Faulk at col. 30, lines 34 - 41 is the voltage Vcc, a supporting voltage for components, not an output voltage.

Independent claim 13 states:

(c) the secondary circuit voltage sensing control circuit being responsive to the voltage sensed to turn OFF the secondary switch when current in the secondary winding is in a range from substantially zero current and a reverse current level to induce in the primary winding a current level in a range from zero current to a reverse current level to thereby cause, when the secondary circuit voltage sensing control circuit senses an overvoltage condition, energy to be transferred back to the primary winding circuit from the secondary winding circuit at a level depending on the level of over-voltage.

The portion of Faulk cited by the examiner states:

> The presently preferred embodiment includes a bootstrap relation which lets the primary high-voltage source supply the VCC power during the start-up phase, and then disconnects this input-derived power supply.
>
> The presently preferred embodiment includes a self-regulating relationship wherein the primary regulates its own VCC supply.

So Faulk does not teach the technique of output voltage control clearly called for in claim 13. And the Pietkiewicz et al. patent teaches nothing to overcome this failing of Faulk. Since the two cannot be combined to provide what is taught in neither, the outstanding obviousness rejection of this claim and dependent claims 14 - 20 is in error and should be withdrawn.

Claims 28 - 32

Claims 28 - 32 stand rejected as obvious over the Martin patent and the Nagagata et al. U.S. patent No. 4,958,268. The Martin patent is said to be applied in the same fashion as with respect to claims 21 - 27. The Nagagata et al. patent is said to teach the use of reverse current through the semiconductor switch and a predetermined reference voltage lacking in the Martin patent. However, claims 28 - 32 depend from claim 27 which requires that the sensing elements in the first and second circuits according to the invention are current sensing elements. None of claims 28 - 32 call for the "predetermined reference voltage" for which the examiner cites Nagagata et al. It would not have been obvious to combine the two patents to arrive at the current sensing elements since neither patent has such elements.

Claims 33 - 43

Claims 33 to 43 are rejected as obvious over the Martin patent, the U.S. patent to Kondo, No. 6,151,233 and the U.S. patent to Taurand, No. 5,745,351. The Martin patent is said to be applied in the same fashion as it is applied to claims 21 - 27. However, independent claim 33 is very unlike claim 21. The Kondo patent is said to teach the detection of the direction of current through a semiconductor switch and the Taurand patent is said to teach the use of "zero current" (apparently zero current switching) and "overload protection." The Kondo patent does not teach detection of the direction of current in a semiconductor switch, it prevents reversal of current in the inductor 12 by predicting that reversal is about to occur. So even if the Kondo controller

applied to a converter with a transformer, which is unlike the Kondo circuits, it would not effect the transfer back of energy to the primary by virtue of the current reversal, but would in fact prevent that happening. Consequently use of the Kondo current detecting scheme would not be obvious in a converter of the kind shown by Martin.

Kondo was cited in the previous Official Action for the teaching alleged here. In applicant's response it was clearly shown that Kondo teaches no such thing.

As for the Taurand patent, this too was discussed in applicant's previous response. The same Taurand specification section, column 18 lines 35 - 70, was cited in the previous Official Action similar to its employment in this Official Action. The misperception of that section was pointed out in the previous Response and applies here as well.

The Kondo patent describes a synchronous rectifier circuit with a high efficiency even in low load conditions (col. 1, lines 5 - 12). Under light load the switch 11 is typically cut off and switch 15 is closed. The current detector 22 senses the current I_L and sends a signal to the control circuit 21 to cut off switch 15 if the current I_L starts being reversed. Then the current I_L may not become negative and the efficiency can be kept high.

Contrary to the invention as claimed in claims 1 - 20 and 33 - 42, Kondo teaches to sense the current through the inductor 12, but does not disclose current sensing means to sense the current through the switch 11. This document is therefore not relevant regarding the invention claimed. It could not be combined to arrive at the claimed invention.

In regard to claim 33, it is not understood why the Kondo and Taurand patents are cited (incorrectly) for reverse current detection and zero current switching as neither is called for in claim 33. The three cited references cannot be pieced together to come up with the DC-DC converter of claim 33, even using claim 33 as a guide. The rejection of claim 33 is in error and should be withdrawn.

As for independent method claim 34 nothing in the Martin and Kondo patents teaches the steps of turning on each of two semiconductor switches when voltage across respective windings is zero and current in each switch and its respective winding is reverse. Kondo teaches away from this, as discussed above. Applying Kondo's teachings to the circuit of Martin would

prevent operation as called for by claim 34. As far as the Taurand patent is concerned, note that Taurand does not provide a "first control circuit for turning ON and OFF the first semiconductor switch solely on the basis of operating parameters in the first circuit" or "second control circuit for turning ON and OFF the second semiconductor switch solely on the basis of operating parameters in the second circuit." (Emphasis supplied.) So the three patents do not teach, and cannot be combined, to arrive at the method of claim 34. The rejection is in error and should be withdrawn.

Claim 35, dependent from claim 34, is patentable by its dependency. In addition the features of claim 35 are not present in any art of record. The rejection of this claim is in error and should be withdrawn.

Independent method claim 36 calls for "detecting by current sensing means in the second circuit when there is a reverse current through the second semiconductor switch" and "turning ON the second semiconductor switch while current therethrough is in a range from zero current to a level of reverse current and when voltage across the second semiconductor switch is substantially zero." As discussed above these steps are not performed in any of the art of record. The rejection of this claim is in error and should be withdrawn.

Claims 37 - 42 are dependent from claim 36 and are patentable by reason of their incorporation of claim 36's steps. The rejection of these claims should be withdrawn.

Likewise method claim 43 calls for, inter alia, "turning ON the second semiconductor switch when the first voltage bears a predetermined relationship to the reference voltage and when a reverse current is sensed in the second semiconductor switch." As discussed above, these features are not present in the prior art. The rejection of this claim is in error and should be withdrawn.

Conclusion

In view of all of the above this application is allowable over the art of record and favorable further examination and allowance is requested.

A three month extension of time in which to respond to the outstanding Official Action is requested in the accompanying Request for Extension and a check for the $1,050.00 extension fee is enclosed. Authorization is given to charge any additional fees associated with this communication to Deposit Account No. 070135. A duplicate copy of this sheet is enclosed.

Should the examiner have questions, comments or suggestions regarding this application, the examiner is invited to please contact the undersigned at the telephone number of email address listed below.

Respectfully submitted,

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